# Deep Dive Into Chips JU and 2025 Calls

**Anton Chichkov,** Chips JU

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# Chips JU

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# A one-of-a-kind Partnership for Europe's Chips Industry

- Chips JU is a tri-partite public-private partnership, established in 2023, as a successor to Key Digital Technologies JU (KDT JU) to advance nano-electronic chip technologies in Europe
- Funded by the European Union, Participating States, and Private Members

## CHIPS JU TRI-PARTITE STRUCTURE


**Private Members**
Industry Associations


**European Union**
European Commission


**Public Authorities**
Participating States

# ECS R&I Calls

## Innovation along the entire value chain

- Focus topics covering AI, cybersecurity, high-performance computing (HPC), semiconductors, and more.
- Chips Joint Undertaking is aligning global research initiatives with European priorities.
- Chips JU is bridging together industry, academia, and policymakers for impactful results.
- It enables large-scale projects with EU and international investment.

€ **1.3 billion**



# The Chips Act: Europe's Lifeline

## Capacity Building through the Chips Act

- **Chips Act:** one of Europe's largest industrial policies aimed at increasing Europe's share of global chip production.
- Chips JU implements the main part of the first pillar of the Chips Act, the **Chips for Europe Initiative**.
- Chips JU acts as a facilitator for public-private partnerships, ensuring that the necessary funding is directed toward strategic projects.
- It aligns the goals of the EU, its Member States, and the private sector. This **tri-partite structure** enables coordinated efforts in semiconductor innovation and capacity building in Europe.

€ **2.8 billion**

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# Role of the three Industry Associations

Aeneas

EPoSS. European Association on Smart Systems Integration

Inside Industry Association

Shape strategic priorities through **Strategic Research and Innovation Agenda (SRIA)**

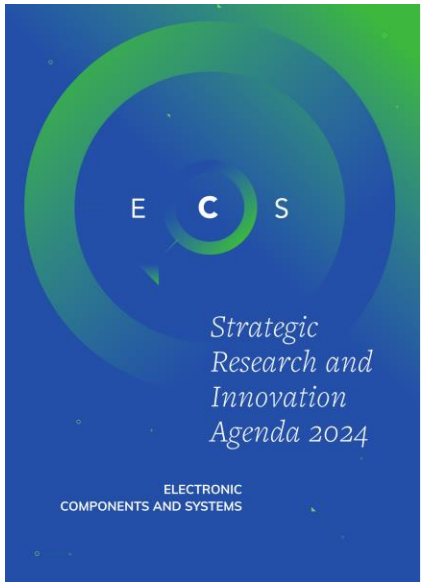
## Key benefits of joining an IA

**Influence future funding calls through the Chips JU Governing Board**

**Influence the Strategic Research and Innovation Agenda (SRIA)**

**Expand your network within the semiconductor ecosystem**

**Gain visibility in shaping future calls and projects**




Chips JU

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# How our selection process works

| Different from usual Horizon Europe (HE) grants | Process – quick overview |
|---|---|
| • Technical evaluation by external experts<br>• National funding availability is a key criterion | • Proposal submission<br>• Expert review<br>• **Funding check by national agencies**<br>• Final selection by Public Authorities Board |

**741 beneficiaries** in 2023

**31%** of participants were **SMEs**

**23% of EU funding** allocated to **SMEs**

**41%** of the **participants** were **newcomers**

On average **40 patents and 120 new innovations brought** to market **annually**

# ECS Calls 2025

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# Chips JU Calls for Proposals in 2025

- Call for Innovation Actions
  - Three topics: Global bottom-up topic (based on SRIA) and 2 focus topics
  - Two stage call
  - With national contribution
- Call for Research and Innovation Actions
  - Single topic: Global bottom-up topic (based on SRIA)
  - Two stage call
  - With national contribution
- Call for Innovation Actions
  - Single topic
  - One stage call
  - With national contribution
- Call for Coordination and Support Action
  - Single topic
  - One stage call
  - Without national contribution

# Chip JU Calls, Topics and Budgets 2025 ECS

| Call | Topic | Maximum JU Budget (M€) |
|---|---|---|
| **HORIZON-JU-Chips-2025-IA** | Global call according to SRIA 2025 | **70** |
| HORIZON-JU-Chips-2025-IA FT1 | RISC-V Automotive Hardware Platform | **80** |
| HORIZON-JU-Chips-2025-IA FT2 | AI-assisted Methods and Tools for Engineering Automation | **20** |
| **HORIZON-JU-Chips-2025-RIA** | Global RIA call according to SRIA 2025 | **40** |
| **HORIZON-JU-Chips-2025-IA-HPA** | Heterogeneous integration for high-performance automotive computing | **20** |
| **HORIZON-Chips-2025-CSA** | Boosting R&I cooperation between EU and Japan on semiconductors | **1** |
| | **Total** | **231** |

# JU Funding Rates

| Call | Large Industry | SME | Other |
|---|---|---|---|
| IA Global | 20% | 30% | 35% |
| IA Focus Topics | 25% | 35% | 35% |
| RIA Global | 25% | 35% | 35% |
| IA Heterogeneous integration for HPAC | 25% | 35% | 35% |
| CSA | 100% | 100% | 100% |

The JU funding rates are complemented by the respective national funding rates

# Chips JU IA proposals

An IA proposal is characterized by:

- The activities have their centre of gravity at the **TRL 5-8.**
- Execution by **an industry led consortium**
- Developing **innovative technologies and/or using them in innovative ways**
- Establishment of a new and realistic innovation environment **connected with an industrial environment,** such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- IA Prjects should contribute to, short to midterm **economic value creation** in Europe

# Focus topic on RISC-V Automotive Hardware Platform

- The overall ambition of this call is to develop in-vehicle demonstrators capable of PetaOPS computing taped-out on leading-edge processes. Proposals are expected to significantly bolster the development of a high-performance automotive RISC-V reference hardware platform, encompassing the following crucial components:
  - **High-Performance RISC-V Automotive Application Processors:** Launch of high-performance, RISC-V application processors designed for automotive applications.
  - **AI and ML Automotive Accelerators:** Development of AI and ML accelerators with specialised ISA extensions for efficient data-intensive computations.
  - **System Integration and Interfacing:** Establishment of a coherent system architecture integrating RISC-V cores, AI accelerators, memory and system peripherals.
  - **Software Tools and Libraries:** Development of a comprehensive tool-chain to support the developed RISC-V hardware.
  - **Collaboration with the Software Defined Vehicle Initiative:** Strengthening of the open-source ecosystem through collaboration between hardware and software development, and automotive industry stakeholders.
  - **Benchmarking and Quality Assurance:** Implementation of benchmarking techniques to assess the performance, safety, and security of the RISC-V platforms.

# Focus topic on AI-assisted Methods and Tools for SDV Engineering Automation

- The project is expected to contribute to the following outcomes:
  - **Advanced AI-assisted methods and tools**, including generative AI, for the automation of software engineering tasks, from enhancing human efficiency and optimizing resource utilization to enabling complex data/problems analysis/interpretation and supporting intelligent decision-making.
  - **Open and extensible AI-assisted integrated platform**
  - **Showcasing and evaluation** for software-defined vehicles of efficiency enhancements in terms of cost and time for complex data/knowledge management, resource optimization, energy consumption, interoperability, product/process quality/trustworthiness, learning curve and usability, over the whole lifecycle, from design, through deployment, operations, and maintenance, to the product end-of-life and recycling, and its evolution.
  - **Best practices and small proof-of-concept studies for other sectors**, e.g. medical/pharmaceutical and/or digital industry.

# Chips JU RIA proposals

- RIA proposal is characterized by
  - The activities have their centre of gravity at **TRL 3-4**
  - Execution normally by an **academy led consortium**
  - Developing **innovative disruptive technologies**
  - Targeting **demonstration of the innovative approach**, clearly addressing relevant societal challenges
  - Demonstrating **value and potential in a realistic lab environment** reproducing the targeted application
  - Having a **deployment plan showing the valorisation for the ECS ecosystem** and the contribution to the Chips JU goals and objectives

# Restricted Calls - Background

- In addition to the standard eligibility conditions, certain calls for proposals may further restrict participation (‘restricted calls’) to:
  - legal entities that are established in eligible countries
  - and/or legal entities that are established in eligible countries and controlled by eligible countries/eligible country entities
- These restrictions apply for duly justified security or strategic autonomy reasons, where they are necessary to protect strategic interests, essential security and/or defence interests of the Union and/or its Member States or to maintain public order and public security
- The calls that are subject to such restrictions and the precise conditions for each call are set out, in the respective Work Programmes

# Legal Basis for Restricted Calls HE Regulation

- **Art. 22(5)**

- For actions related to Union strategic assets, interests, autonomy or security, the work programme may provide that the **participation can be limited to legal entities established only in Member States or to legal entities established in specified associated or other third countries in addition to Member States**

- For duly justified and exceptional reasons, in order to guarantee the protection of the strategic interests of the Union and its Member States, the work programme may also **exclude the participation of legal entities established in the Union or in associated countries directly or indirectly controlled by non-associated third countries or by legal entities of non-associated third countries from individual calls for proposals, or make their participation subject to conditions set out in the work programme**



16

# Chips WP 2025 Topics Under Art. 22(5)

- **ECS topics**
  - HORIZON-JU-Chips-2025-IA
    - HORIZON-JU-Chips-2025-IA FT1
    - HORIZON-JU-Chips-2025-IA FT2
  - HORIZON-JU-Chips-2025-RIA
  - HORIZON-JU-Chips-2025-IA-HPA
- **Chips for Europe inititive topics**
  - HORIZON-JU-Chips-2025-IA-EDA
  - HORIZON-JU-Chips-2025-SGA-QAC1
  - HORIZON-JU-Chips-2025-SGA-QAC2
  - HORIZON-JU-Chips-2025-FPA-QAC3



17

# Chips WP 2025 Art. 22(5) Restrictions

- Restriction of participation to Chips JU Work Programme 2025 topics under Art. 22(5) of Horizon Europe Regulation
  - Subject to restrictions for the protection of European communication networks
  - Participation is limited to legal entities established in **EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries**
  - In order to guarantee the protection of the strategic interests of the Union and its Member States, **entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not participate in the action** unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic assets, interests, autonomy, or security

# Ownership Control Declaration

- The participants that must undergo an ownership control assessment must fill in the ownership control declaration, annexed to the application form.
- This declaration must be signed by a person empowered to represent the legal entity.
- The coordinator must combine all declarations into one single document and submit it with the proposal (signed originals should be kept on file by the participants).
- Proposals missing this annex for any of their participants may be declared inadmissible.
- Public bodies are exempted from this obligation, but they will automatically be considered as controlled by their country. Formal validation in the Participant Register is required; ‘declared’ status is not sufficient.

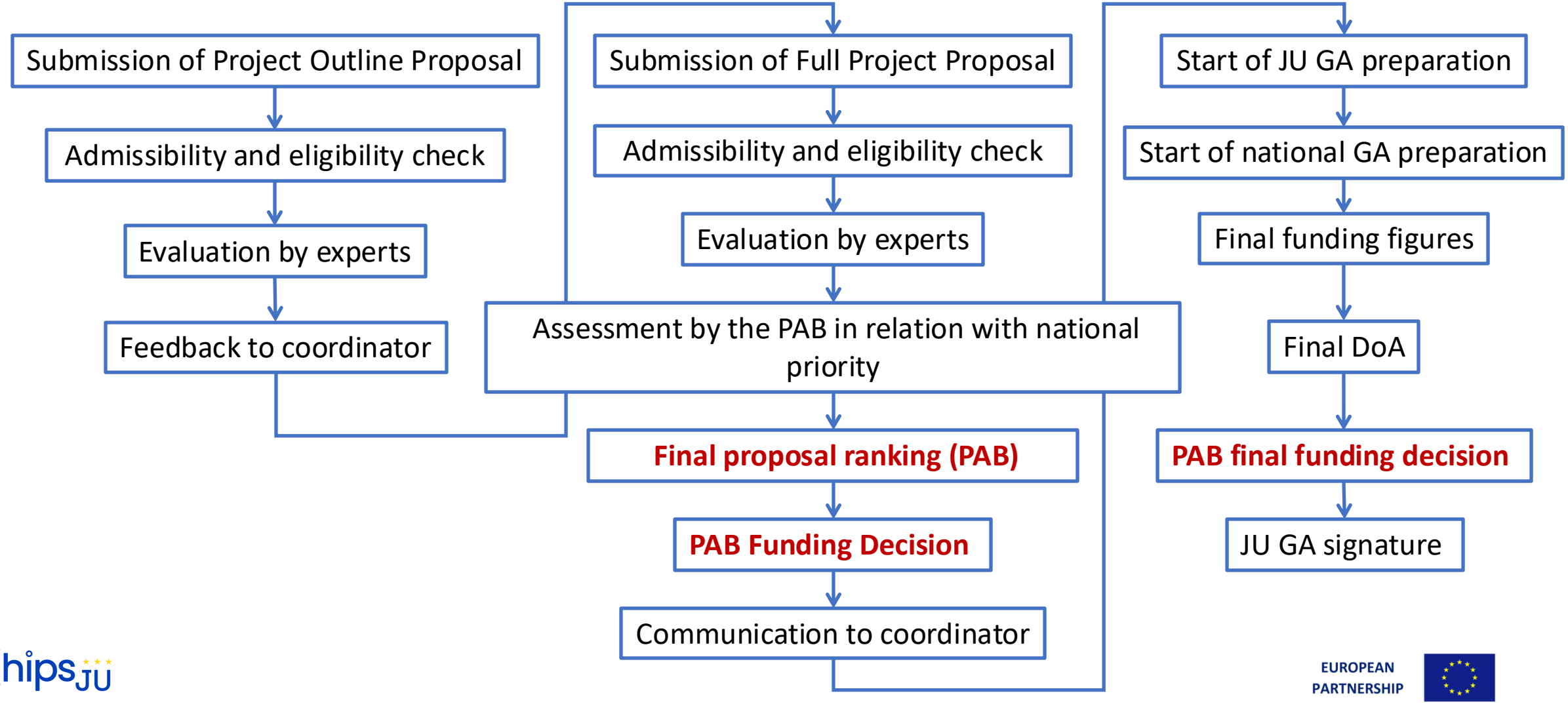
# Guarantees

- In the case of EDF and DEP, if control is established in the context of the ownership control assessment check, you have to provide the guarantees, accompanied by the approval of your country of establishment (eligible country).
- For HE, if control is established in the context of the ownership control assessment check, you will have to provide the guarantees during grant preparation. The granting authority will contact the national authorities of your country of establishment (eligible country) on the assessment of the guarantees and seek their confirmation.

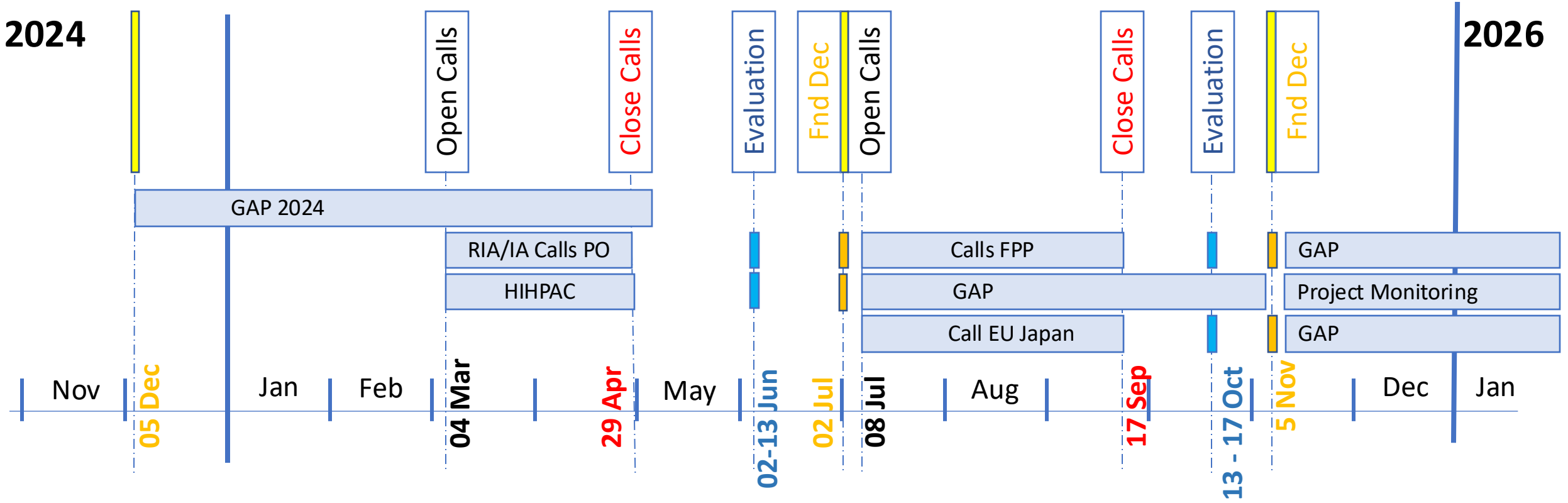
# If the Outcome is ’Controlled’

- If the outcome of the ownership control assessment is ’controlled’, the consortium will be asked to replace the participant concerned (or redistribute the tasks between the other participants). If this is not possible and the consortium cannot propose any other acceptable solution, the proposal will have to be rejected.
- Only solutions that do not imply substantial changes to the proposal can be accepted (solutions that — if they had been known — would have impacted the evaluation result can NOT be accepted).

# Proposal Evaluation, Selection, and Grant Agreement Preparation



# Planning Calls 2025 ECS



# Chips for Europe  Calls 2025

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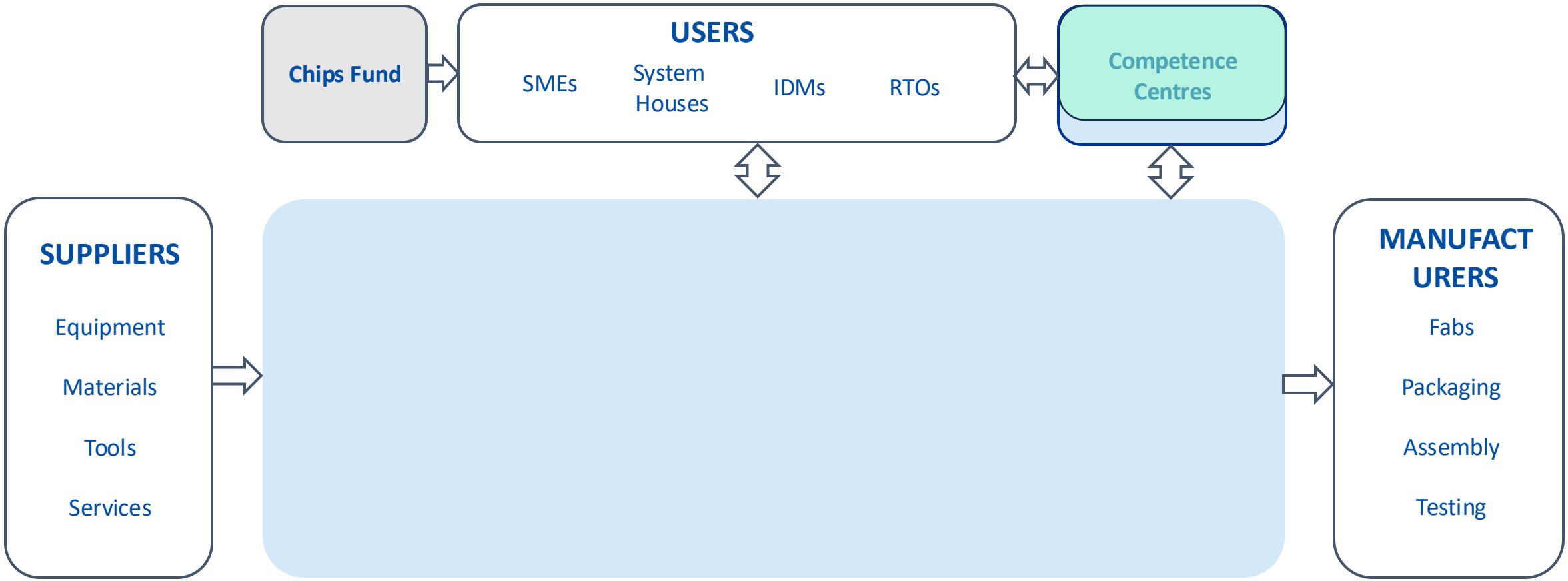
# Ongoing Activities Chips for Europe Initiative Part

| Chips for Europe Initiative | HE Budget | DEP Budget |
|---|---|---|
| **Operational budget** | **1,417 M€** | **1,373 M€** |
| Signed contracts | 761 M€ | 720 M€ |
| In preparation | 133 M€ | 331 M€ |
| **Total** | **894 M€** | **1,051 M€** |

# Chips for Europe Initiative



# Pilot Lines

- NanoIC

  The overall objective of the NanoIC project is to set up and give access to a 300mm pilot line to the entire semiconductor ecosystem to advanced, beyond 2nm system-on-chip technologies.

- FAMES

  With the goal of transferring results to the EU semiconductor industry, the FAMES Pilot Line will develop advanced technologies offering 2 generations of FD-SOI at 10nm and 7nm nodes.

- APECS

  Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems Pilot Line (APECS-PL).

- WBGPL

  WBGPL aims to realise an integrated pilot line focused on the developments of the wide–bandgap (WBG) semiconductors technologies for power and radio frequency (RF) electronics. PIXEurope

- PIXEurope

  PIXEurope will establish a globally unique Open Access Pilot Line, addressing key technological and production challenges associated with Photonic Integrated Circuits (PICs)

# Competence Centres & Design Platform

- CCC1

  Have specialised areas of expertise in certain technology, domain, or activities (specialisation). Facilitate effective use of capacities and facilities, including access to design platform and pilot lines. Support interested stakeholders in developing semiconductor solutions (technology transfer). Address skills shortage by offering (access to) training on semiconductors, including workforce upskilling and reskilling. Match user needs with available expertise in network of competence centres and act as access point to the network, Awareness raising, promoting services, promoting success stories

- CCC2

  Targeting the establishment of European Network of Chips Competence Centres (ENCCC)

- CCC3

  Additional call for competence centers for countries that did not submit in the first call

- PCT

  The DECIDE project aims to create a virtual design platform to democratize access to advanced semiconductor technologies across Europe. This platform will support the innovation and competitiveness of European startups, SMEs, and research institutions. By integrating Design Enablement Teams (DETs), the platform will offer customized support, access to Electronic Design Automation (EDA) tools, intellectual property (IP), and pilot line technologies, helping Europe to deploy next-generation semiconductor technologies rapidly

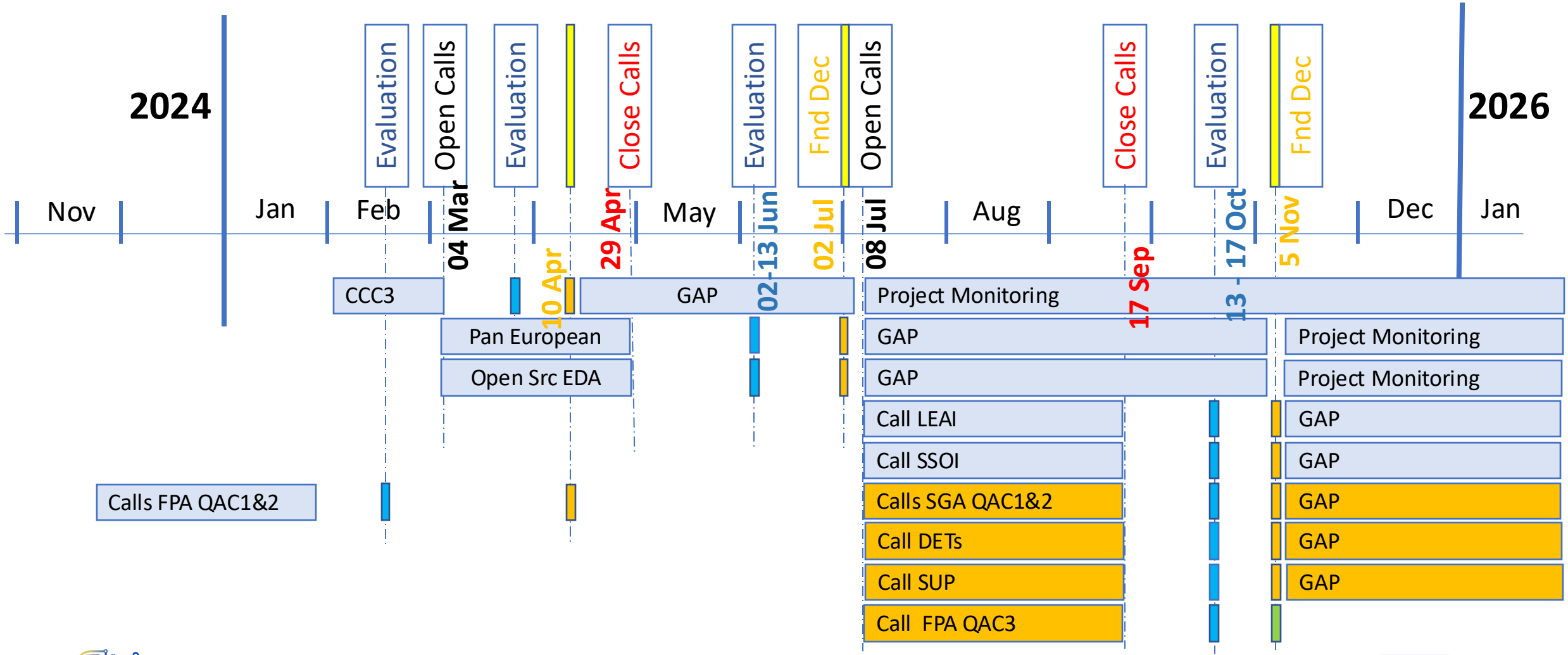
# HE Actions 2025

| Topic | Description | Indicative JU Budget M€ |
|---|---|---|
| HORIZON-JU-Chips-2025-RIA-SUP | Support for start-ups and SMEs | **220** |
| HORIZON-JU-Chips-2025-CSA | Pan-European infrastructure for Chips Design Innovation | **12** |
| HORIZON-JU-Chips-2025-IA-EDA | Open-source EDA tools development | **20** |
| HORIZON-JU-Chips-2025-FPA-QAC3 | Establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots | **0** |
| Lab to Fab | Lab to Fab accelerator European ecosystem for chiplet integration | **50** |
| **Other Activities** | | |
| HORIZON-JU-Chips-2025-SGA-QAC1 | Supporting developing Quantum Chip Technology for stability Pilots | **50** |
| HORIZON-JU-Chips-2025-SGA-QAC2 | Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot | **20** |
| **TOTAL** | | **372** |

# DEP Actions 2025

| Topic | Description | Indicative JU Budget M€ |
|---|---|---|
| Call for tenders | Cloud platform for the European Design Platform | **15** |
| DIGITAL-JU-Chips-2025-CSA-DET | Set-up and integration of Design Enablement Teams | **5** |
| DIGITAL-JU-Chips-2025-SG-SSOI | Accelerator for Advanced Strained Silicon on Insulator Substrates | **30** |
| DIGITAL-Chips-2025-1-IA-LEAI | Low-power Edge AI Chips | **20** |
| **TOTAL DEP** | | **70** |
| **TOTAL Chips for EU Initiative 2025** | | **442** |

# Planning Calls 2025

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